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A COMPARATIVE STUDY AND ANALYSIS OF FULL ADDER

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ABSTRACT

In Electronics adders are used widely. An adder performance is analysed using trems delay and power comsumption. This paper contains various adders simulated using Mentor graphics in180 nm technology and their comparsion using power delay product.

KEYWORDS: Hybrid adder, PMOS, NMOS.

INTRODUCTION

In designing of adders we need to concentrate on factors like power consumption, number of transistor, delay. In today time power consumption is very important factor. Adder is a basic building block in digital design .Hence we need to focus on performance of adders so that, overall performance of circuit can be improved.By improving specification like power, number of transistor and capacitance of circuit, overall performance is drastically improved. [1,2]. In digital design three ways of power dissipationareas following :

1.Leakage Power: Power dissipation when transistor is in cut off.
2. Short Circuit Power: When a short circuit exist between applied voltage and ground.
3. Switching Power: Due to continuous charging and discharging of capacitance in circuit..

There are 6 chapter sections. Chapter I deals with basics of adder. Second chapter contains previous adders with their merits and demerits. In chapter three, adder with less number of transistor are explained.In chapter IV and V discuss new approach and comparison with already present.

ADDER

For addition of two numbers addersare used. Oldest technology uses static CMOS for adder as Fig. 1. Its merits are easy design, small voltage to operate and comfortable in resizing the transistor [3]. Static CMOS uses same number of NMOS and PMOS, hence more area requirement increases. For this compensation domino logic has been used [4]. Dynamic circuit when design with static circuit then logic is called Domino gate [5] as in Fig. 2. These circuits are faster and less power consumption but are not used for multilevel circuits [6].

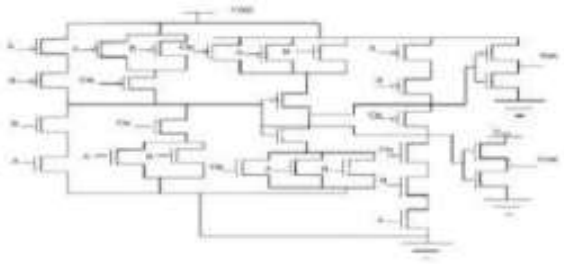

Fig. 1: Static CMOS Adder Circuit.

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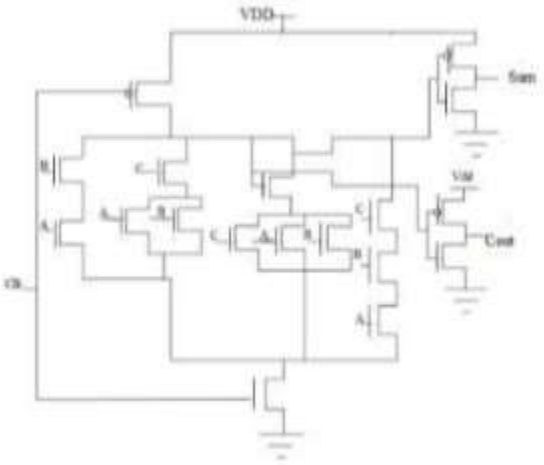

Fig. 2: Domino Logic Full Adder.

LESS TRANSISTOR COUNT TYPE FULL ADDER

Mainly two transistors in this family are 10T and 14T. They require less number of transistors Fig. 3[5]. But they suffer problem of threshold voltage drop.

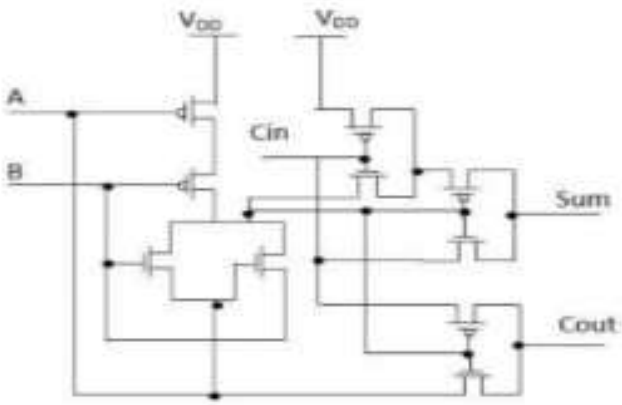

Fig 3:10 T adder circuit.

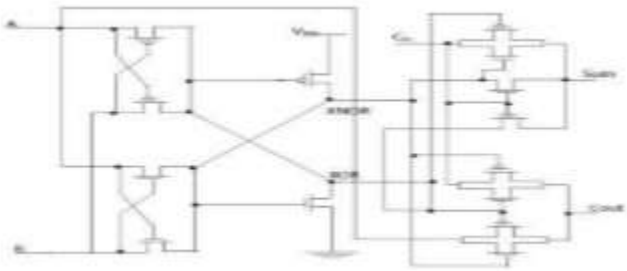

Fig. 4: 14 T Adder Circuit.

Another less transistor count type full adder is 14 T, it requires only 14 transistor.They produce XOR/XNOR function at same time, so delay decreases and power delay product become less.

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HYBRID ADDER AND COMPARISION

Figure 5dictates module 1[8]. Main problem occurs due to threshold voltage drop and due to transition from 01 t0 00.

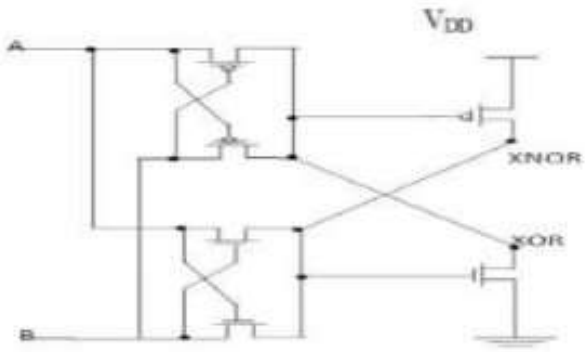

Fig. 5: Module 1 of adder circuit.

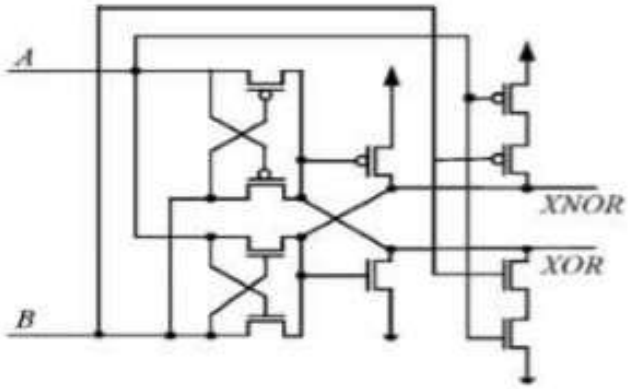

Fig. 6: Modified Module 1 circuit.

Low power response of this circuit is not good. Hence to improve this problem of threshold voltage drop we will now use two transistor i.e. PMOS and NMOS in series as given in figure 6, it is called modified module 1. They will solve problem of transition of 01 to 00. By doing so full voltage will be made available at output. Hence less power is dissipated,inmodule 2 contains multiplexer to select sum or carry outputin Fig. 7 and 8 respectively. The results and performance are given and compared.

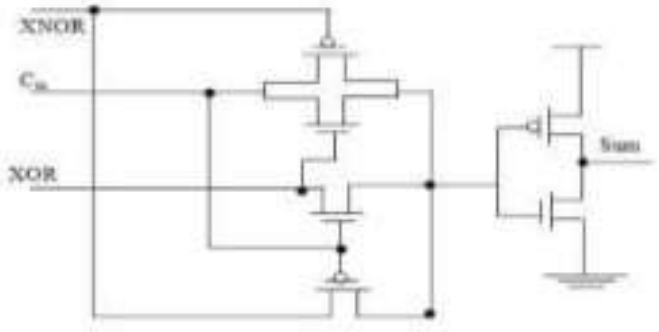

Fig. 7: Module 2 for adder circuit.

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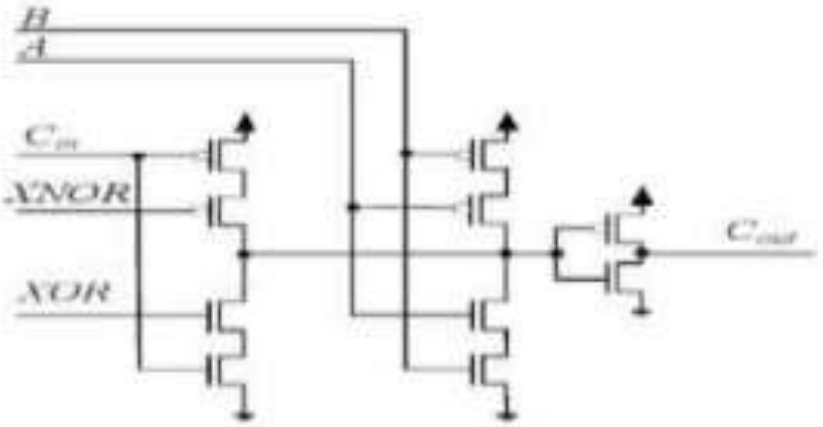

Fig.8: Module 3 for adder circuit.

By using multiplexer carry output is in module 3 [10]. Combining all three modules of adder as in Fig.9.

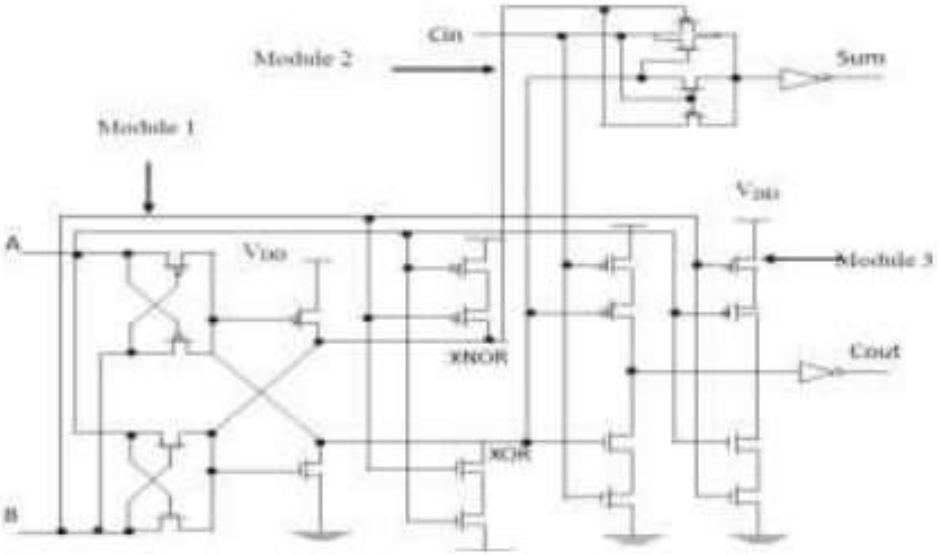

Fig. 9: Modified Hybrid full adder.

Table 1:Analysis of existing adders

Adder Name	Power	charctrtics Delay	PDP
Static CMOS	16.727	119.769	1932.435
Domino	17.816	155.521	2303.311
10 T	13.621	116.336	1389.312
14 T	9.001	114.218	817.028
HYBRID	6.689	117.019	620.952

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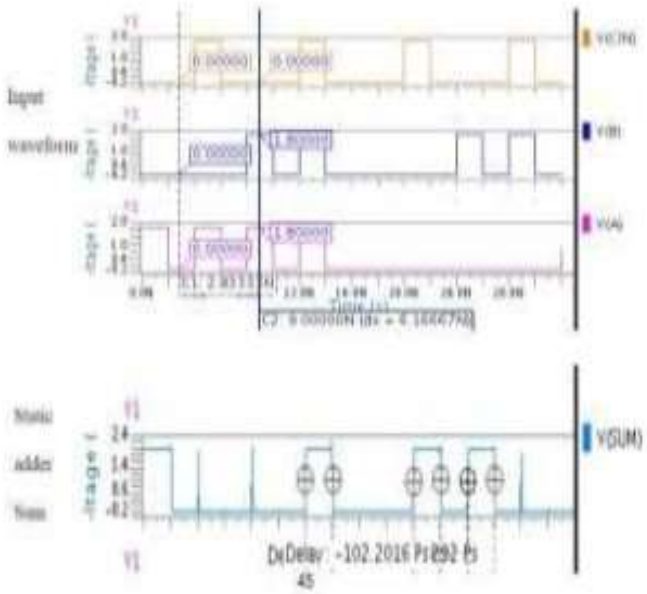

Fig. 10: Output waveforms depicting delay.

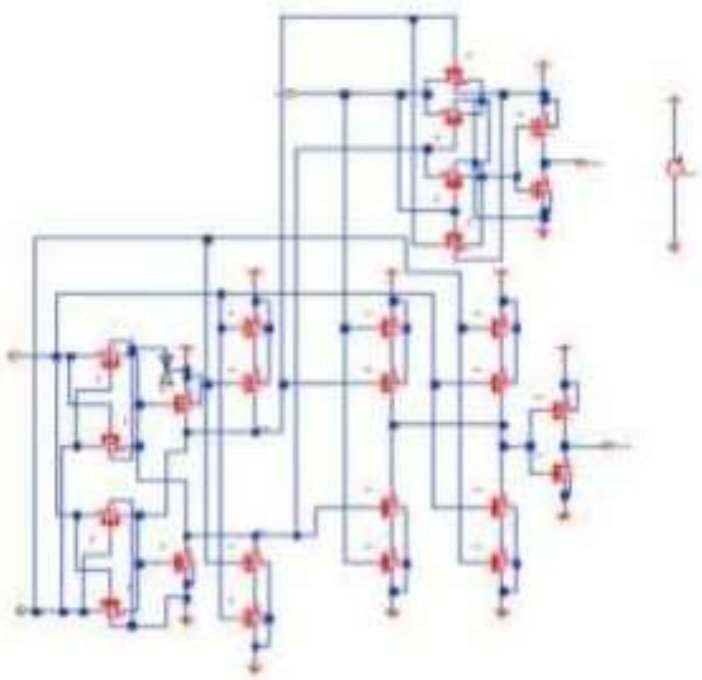

Fig. 11: Modified Hybrid Full Adder.

CONCLUSIONS

Adder are most widely used in low power VLSI, microprocontroller etc. complete study of all previous adder and newly hybrid adder is done in this paper also from result obtained it is clear that newly designed adder consumed less power and hence more efficient capability of new hybrid adder is better. For applications where less power delay product is required our new designed adder is more efficient and can be used .

REFERENCES

[1] S. F. Frutaci, M. Lanuzza, P. Zicari S. Perri, P. Corsonello " Low Power Split Path Data Driven Dynamic Logic" published in IET Circuit Devices & Systems 20th April 2009
[2] Jin-Fa Lin, Yin-Tsung Hwang, Ming-HwaSheu, "A novel high- speed and energy efficient 10-transistor full adder design" IEEE Transactions on circuits and systems Vol. 54 No. 5, May 2007.
[3] M. Alioto and G. Palumbo, "Analysis and comparison on full adder block in submicron technology," IEEE Trans. Very Large Scale (VLSI)Syst., vol. 10, no. 6, pp. 806–823, Dec. 2002
[4] Mark Vesterbacka "A 14-transistor cmos full adder with full voltage swing nodes" Proc. Int. Symp. On circuit and system, Vol. 1, pp-49-52,1999.
[5] Amir Ali Khatibzadeh, KaamranRaahemifar, "A study and comparison of full adder cells based on the standard static CMOS logic" Proceedings of the International Symposium on Low Power Design, 2004.
[6] R. Rafati, S. M. fakhraie, K. C. Smith, "Low-power data-driven dynamic logic" IEEE International Symposium on circuits and systems, May 28-31, 2000.
[7] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," Proc. IEEE Circuits, Devices and Systems, vol. 148, no. 1, pp. 19–24, Feb.2001..
[8] Amir Ali Khatibzadeh, KaamranRaahemifar, "A study and comparison of full adder cells based on the standard static CMOS logic" Proceedings of the International Symposium on Low Power Design, 2004.
[9] G. Sathaiyabama, Raja Shailaja, "A survey of Low power High Speed Full Adder", vol 2 issue 9, sep 2012.
[10] N.Weste and K. Eshraghian, Principles of CMOS VLSI Design, A System Perspective. Reading, MA: Addison-Wesley, 2011.